

**AMENDMENTS TO THE CLAIMS**

This listing of the claims replaces all prior versions, and listings, of claims in the application:

**LISTING OF CLAIMS**

1. (Cancelled)
2. (Cancelled)
3. (Cancelled)
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- 35. (Cancelled)
- 36. **(Original)** A system for extracting design and layout information from a plurality of image-mosaics representative of a deconstructed integrated circuit, the system comprising means for enabling parallel design analysis of the image-mosaics by a plurality of engineer analysts concurrently reverse engineering an IC.
- 37. **(Original)** A system as claimed in claim 36, wherein the plurality of image-mosaics are annotated concurrently using a plurality of design analysis workstations.
- 38. **(Original)** A system as claimed in claim 37, wherein each one of the annotation objects created using a design analysis workstation participating in parallel design analysis includes an ownership attribute specifying an engineer analyst associated with the design analysis workstation at a time when the annotation object was created.
- 39. **(Original)** system as claimed in claim 38, wherein annotation objects include an identification string, and the system further comprises means for generating unique identification strings.
- 40. **(Original)** A system as claimed in claim 38, wherein annotation objects having different ownership attributes can be merged for display on one design analysis workstation.
- 41. (Cancelled)

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- 71. (Cancelled)
- 72. **(Original)** A method of analyzing a design of a deconstructed integrated circuit using a design analysis workstation, comprising a step of propagating signal information from an annotation object having a signal property to at least one connected annotation object.

73. **(Original)** A method as claimed in claim 72 further comprising a step of propagating signal information between a cell and a wire annotation object.
74. **(Original)** A method as claimed in claim 73 further comprising a step of generating a net-list from interconnected cells.
75. **(Original)** A method as claimed in claim 72, wherein propagating signal information further comprises steps of:
- a) selecting all contact annotation objects connected to a wire annotation object, the wire annotation object and the contact annotation objects having at least one specified layer in common; and
  - b) propagating signal information from the wire annotation object to all annotation objects connected to the contact annotation objects.
76. **(Original)** A method as claimed in claim 75 further comprising a step of detecting a logical short if two different signals are propagated to a given annotation object.
77. **(Original)** A method as claimed in claim 76, wherein on detecting the logical short the method further comprises a step of displaying information about the logical short on the design analysis workstation.